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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,103	11/01/2001	Paul D. Nuber	10011002-1	9982

7590 12/26/2003

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EXAMINER	
BENENSON, BORIS	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 12/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,103	NUBER ET AL.	
	Examiner	Art Unit	
	Boris Benenson	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Detailed Actions

1. Amendment received on 11/03/2003 is entered. Claims 2 and 3 are canceled. Claims 1, 4-13 and 16-18 are amended. New Claim 21 is entered.

Response to the arguments

2. Applicant's argument related Claims 14 and 20 is convincing even it has some elements of tautology. It indicates that all manufacturing processes are include preselection, because a manufacturer know sizes and parameters of elements prior to manufacturing and in such case limitation of the claims include all kind of manufactured products. Nevertheless with such broad interpretation of word "preselection" it cannot be given a patentable weight.

Applicant argue (page 7, 3rd paragraph of remarks) that the application describes an invention that is "process independent and can be applied regardless of the IC process used to create the IC…" and (page 8 of the same paragraph) that the present invention is process-dependent and vendor-dependent. That argument is confusing. Applicant indicates that the specification has been amended to specifically refer to BJT process technology. That amendment had not been received and need to be resubmitted. Amended Claim 6 does not have limitation requiring use of bipolar

transistor (BJT) technology. Rejections under 35 USC § 112 first paragraph are withdrawn.

3. Applicant's argument that the phrase "at least partially dependent" is clearly supported in the specification is convincing. Rejections under 35 USC § 112, second paragraph are withdrawn.

4. Applicant argues that Claims 1 and 10 require the protection diode to be included in the buffer itself and this inclusion was newer disclosed in Prior Art, including Applicant's Admitted Prior Art. Applicant indicates that inclusion of the protection diode in structure of the buffer is not simple integration of parts, but eliminates known problem, because it allow to place the diode in proper location without limiting the diode effectiveness. That statement is correct, but rejection is based on reason that claim language does not specifically require *the protection diode to be located inside an integrated circuit (IC) comprising a buffer used to reduce delay on relatively long conductive signal lines*. The claim language is only requiring "a protection diode connected to the input of the first inverter".

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 6 and 15 recite the limitation bipolar junction transistor (BPJ). There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1,10 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant admitted Prior Art. The specification stated, "the inclusion of buffers along long lines is relatively common in ICs manufactured using current IC manufacturing processes" (Page 1, Lines 20-22). The specification also stated (Page 1, Lines 27-30): " One known solution to this problem is to fabricate diodes into the IC that are coupled to the lines at locations close to

the buffers. The diode will pull enough of the charge off of the gate of the FET to prevent damage to the FET, and thus to the buffer."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 5,10-12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (5,969,929) in view of Sigal (5,910,730). Kleveland et al. disclose a distributed ESD protection device for high speed integrated circuits that comprises a buffer (Fig.2C, Pos.248) having input and output, a protection diode (254) coupled to input of the buffer, wherein the protection diode dissipates a part of an electrostatic charge to the ground to prevent a damage of the buffer. Kleveland et al. didn't disclose the buffer's circuitry. Sigal teaches a non-inverting buffer (fig. 2b) formed by combining two logic inverters. Sigal teaches that each inverter "consists of a PFET (Fig.2a, Pos. 204) and an NFET (Pos. 208) connected in a common drain configuration between the positive power rail (Pos. 210), VDD and the negative power

rail (Pos. 212), ground. The gate inputs of both transistors are tied together to form the inverter input (202). The signal at the output (206) is the logical complement of the signal at the input (202)" (Col.5, Line 63 - Col.6, Line 2). It would have been obvious to one of ordinary skill in the art at the time the invention to use Sigal's teachings when designing a non-inverting buffers circuitry, because such buffer will help to reduce a delay on a line without changing the polarity of the input signal.

Referring to Claims 11 and 12, Kleveland et al. disclose inclusion of a protection diode into each element of the conductive signal line. I would have been obvious to one of ordinary skill in the art at the time the invention to protect each buffer and exclude such protection, if it had been determine to be unnecessary.

Referring to Claims 5 and 16 the buffer disclosed by Sigal meet all limitation of the Claims.

9. Claims 4,7,8,13,17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (5,969,929) in view of Sigal (5,910,730) as applied to claims 1 and 10 above, and further in view of Shiota (5,426,322). Kleveland et al. (5,969,929) in view of Sigal (5,910,730) disclose all the limitations of claims 1 and 10, but silent about a size of the protection diode. Shoat teaches, " the actual protection by a diode … is dependent

on the size of protection diode, with larger diodes capable of absorbing larger amounts of charge" (Col.4, Lines 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention that parameters of a gate area of the transistor gates of the buffer and dimensions of the conductive signal line to which the buffer input is connected will define overall charge from which an IC should be protected and teachings of Shiota should be taken in a consideration so parameters of the protection diode for the circuitry disclosed by Kleveland et al. (5,969,929) in view of Sigal (5,910,730) will at least partially depend on dimensions of the conductive signal line and gate area of transistors, because only proper size of the protection diode will protect the IC from possible ESD inflicted damage.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (703) 305-6917. After 1/28/2004 telephone number will be changed to (571) 272-2048. The examiner can normally be reached on M-F (8:20-6:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. After 1/28/2004 telephone number will be changed to (571) 272-2058. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Boris Benenson
Examiner
Art Unit 2836

B.B.

Stephen W Jackson
12-23-03

STEPHEN W. JACKSON
PRIMARY EXAMINER